Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1.-6. (CANCELED)

7. (ORIGINAL) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

pattering a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are only partially opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

8. (ORIGINAL) The method according to claim 7, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

9. (ORIGINAL) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

pattering a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other, and a distance between the opposing hole patterns is larger at central portions of the respective hole patterns;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

10. (ORIGINAL) The method according to claim 9, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

11. (ORIGINAL) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact

plugs;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film,

wherein the mask pattern is patterned with a pitch of the hole patterns that makes a distance between opposing central portions of the adjacent storage nodes larger than a distance between opposing corners thereof due to proximity effect during formation of the storage nodes.

12. (ORIGINAL) The method according to claim 11, wherein the pitch is smaller than 0.55 μm.

13. (ORIGINAL) The method according to claim 11, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

14. (ORIGINAL) A method for manufacturing a semiconductor memory device comprising:

depositing an interlayer insulating film on a semiconductor substrate provided with contact plugs;

patterning a mask pattern on the interlayer insulating film, the mask pattern having a layout in which a plurality of hole patterns having the same shape are arranged so that the adjacent hole patterns are opposite to each other;

forming holes for storage nodes in the interlayer insulating film by etching with the mask pattern;

forming the storage nodes in the holes so as to be connected electrically to the contact plugs;

etching an upper potion of the interlayer insulating film between the storage nodes;

forming a capacitor insulating film on the storage nodes; and

forming a plate electrode on the capacitor insulating film.

15. (ORIGINAL) The method according to claim 14, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.